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Our Case No. 9799940/0010
Cypress Ref. No. PM95029(2)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
In re Application of James M. Cleeves
Serial No. 08/581,347
Filing Date of December 29, 1995
For: WAFER TEMPERATURE CONTROL APPARATUS AND METHOD))))))
)
)

Appeal no. 2003-1081

37 C.F.R. §1.132 DECLARATION

Commissioner for Patents
Washington, D.C. 20231

Dear Sir,

I, Krishnaswamy Ramkumar ("I" or "Affiant") hereby declare as follows:

1. I am **not** the inventor of the subject matter of the above identified application.

2. I am presently an employee of the sole assignee of the above identified application, Cypress Semiconductor, Inc., and have been since September 30, 1993.

3. From about the end of 1993 through the middle of 1994, I participated in the production of semiconductor devices, including the plasma etching of substrates, for example the etching of a layer of tungsten with fluoride ions in a plasma. After the middle of 1994, I continued to be informed about plasma etching through regular discussions with people at Cypress Semiconductor, Inc. who participated in the production of semiconductor devices, including the plasma etching of substrates.

4. My knowledge of the field of plasma etching in 1995 was typical of people in the field who actually carried out plasma etching.

5. My resume is attached as Exhibit A.

6. I have read the above identified application, including the presently active claims. The field of the invention described in the application is the field of plasma etching.

7. At the time of filing of the above identified application, December 29, 1995, I as well as others in the field, would have understood the phrases "transferring heat . . . substantially uniformly across said substrate . . ." and "substantially uniform heat transfer across said substrate" to mean that the temperature of the substrate would be uniform enough that the etching of different parts of the substrate would not be uncontrollable, or in other words a temperature differences across the substrate of less than 10 degrees Celsius. Similarly, I as well as others in the field, would have understood the phrase "said substrate has a substantially uniform temperature" to mean that the temperature differences across the substrate would be less than 10 degrees Celsius.

8. I have reviewed Patent no. 5,698,070 to Hirano et al. This reference describes the same problem as the above identified application (see, for example, col. 1, lines 25-33). A temperature difference of less than 10 degrees Celsius between different parts of the substrate as being sufficiently uniform that the etching of different parts of the substrate would not be uncontrollable, is consistent with this reference (see, for example, col. 10, lines 1-35).

9. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Krishnaswamy Ramkumar — 9/22/03

Krishnaswamy Ramkumar — Date

EXHIBIT A

Krishnaswamy Ramkumar

1193 Lynbrook Way
San Jose; CA 95129
Ph: (408) 255 - 1031 (Res)
Email: KRamkumar@aol.com

Professional Goal

To contribute significantly to Research and Development of advanced VLSI technology segment of the semiconductor chip industry from a key management position

Professional Career Background

1993 to date:	Process Development Engineer at Cypress Semiconductor, San Jose, working on various aspects of VLSI processing - Oxidations, isolation (LOCOS and STI), gate / tunnel oxide process development, ONO stack development for SONOS, silicide process development, CVD processes, critical precleans, SOI technology, dual gate technology development, low K dielectrics Current designation: **Senior Member of Technical Staff - in charge of Advance Technology Development at Cypress**
1990 to 1993:	Visiting Research Associate at Rensselaer Polytechnic Institute; Worked on characterization of CVD SiO2 films for Multilevel Metallization schemes, interaction with Al lines etc Taught parts of courses on IC fabrication, Semiconductor devices
1989 to 1990	Visiting Scholar at Rutgers University Worked on Ferroelectric thin films and superconductor films
1980 to 1989	Faculty at Indian Institute of Science Guided Masters and Ph.D students on various topics of Semiconductor devices and electronic materials; Taught courses on Semiconductor devices physics, Microelectronics, Instrumentation etc (8 years)

Immigration Status

Permanent Resident

EXHIBIT A

Publications and Patents

Over 75 publications in reputed journals and conferences;
2 Indian patents
9 US patents approved or issued
25 US patents filed

Books

One text book on "Electronic Devices" published by Wiley Eastern Ltd (India) in 1992.

One chapter in the "Hand book of Multilevel Metalization" published by Noyes Publications in 1993.

Educational Background

M. Tech with Electronics specialization; Indian Institute of Science, Bangalore, India, 1976.

Ph.D in Electrical Engineering, Indian Institute of Science, Bangalore, India, 1980

Key technical contributions in the last 6 years

1. Developed process modules for ultra thin tunnel oxide for E^2PROM (growth on highly doped silicon)

2. Led development and transfer to manufacturing of LOCOS isolation for 0.35 um SRAM technology

3. Key contributor to initial development of LOCOS isolation for 0.25 um technology

4. Led the development of Shallow Trench Isolation for 0.20 um technology– extended to 90 nm technology

5. Developed ultra thin gate oxide process modules with precleans– from 150 A to 35 A

6. Process integration of tungsten silicide into SRAM technology

7. Development of dual gate oxide technology for 5 V/ 3.3 V compatible SRAM technology

8. Resident expert on all front end issues at Cypress

EXHIBIT A

9. Involved in development of low K dielectric based metallization

10. Involved in development of TiSi2 and CoSi2 technology

11. Process integration of poly – tungsten gate stack

12. Development of nitrided gate oxide (~ 20 A EOT) in a batch tool

13. Deuterium incorporation for improvement of device reliability

14. Development of in-situ ONO process in a batch tool

15. Defect reduction through substrate engineering

Equipment Related Contributions

1. Successfully implemented a dilute steam oxidation recipe for critical oxides on batch furnaces (Horizontal and VTR) – high quality gate oxides

2. Implemented the Preclean recipes in FSI and Wet Bench - HF last and RCA last

3. Optimization of recipes in FSI for performance and COO

4. Defined configuration and specs for a DNS wet bench for frontend cleans

5. Development of a robust recipe in the DNS start up

6. Optimization of CVD process for nitride deposition for superior particle performance

7. Developed a process/recipe for ONO film deposition in a AVP; incorporated all effects due to pressure, temperature, cooling etc

8. Defined specs and procured the first Optiprobe 2400 DUV for measuring thin films

9. Defined specs and procured the first ASET F5 from KLA for measuring ultra thin film stacks

10. Involved in the selection of the gapfill tool for STI